

## REMARKS

This application has been reviewed in light of the Office Action dated November 29, 2002. Claims 1,2, and 4-9 were rejected under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent No. 5,528,177 ("Sridhar et al."). Claims 2 and 4-6 have been canceled without prejudice.

Referring now to Claim 1, it is submitted that Claim 1 as amended is patentable over Sridhar et al. The Examiner indicates that Sridhar et al. teaches all claimed features in Fig. 2g. Applicants respectfully disagree. Sridhar et al., at Fig. 2g, discloses a logic circuit for performing a logical AND/NAND operation (see Sridhar Col. 11, lines 29-41). To the contrary, Claim 1 recites a logic circuit for performing a logical OR operation. Sridhar et al. does not disclose, teach, or suggest a logic OR circuit, as is recited in Claim 1. For example, Sridhar et al. must use an inverter to achieve a logical OR result. The invention recited in Claim 1 achieves a logic OR result using only three transistors, resulting in a reduced delay and circuit size. To the contrary Sridhar et al. requires a minimum of four transistors, including an inverter, to achieve a logic OR result.

For at least the reasons discussed herein, Sridhar et al. does not disclose, teach, or suggest the logic OR circuit recited in Claim 1. It is respectfully submitted that Claim 1, as amended, is patentable over Sridhar et al. By virtue of their dependence upon Claim 1, it is further submitted that Claims 7-9 are also patentable over Sridhar et al.

In view of the foregoing amendments and remarks, it is respectfully submitted that this case, and all pending claims, are in condition for allowance. Such early and favorable action is earnestly solicited.

Should the Examiner have any questions concerning this communication or feel that an interview would be helpful, the Examiner is requested to call the undersigned at the number indicated below.

Respectfully submitted,



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